WHAT'S IT ABOUT…

The Electronics & Telecommunication Engineering Department of Padre Conceição College of Engineering, Verna, Goa in association with IETE-Student Forum(ISF), is organizing a one week ISTE STTP on **'Cadence- Design, Analysis and Simulation of Circuits.'** VLSI circuit design inherently consists of power, speed and area constraints. With changing market needs, emphasis is shifting towards power aware and high performance circuit designs. With ever increasing transistor integration, new advances are seen in the concerned design strategies and related tools enabling implementation of cost effective, low power high performance VLSI circuits.

In this workshop, the intention is to review the basic concepts of Digital and Analog VLSI circuits and provide complete guidelines for developing UG/PG VLSI projects. The main objective of the course is to imbibe the knowledge of VLSI Design and provide hands on experience on Cadence tools to the faculty members and student community.

This workshop will comprise of lectures delivered by academic and industry experts in the field of CMOS Analog and Digital design. The participants will have an exposure to the Circuit design & Simulation, Layout design, DRC, Physical Verification, Parasitic Extraction, with hands-on session on the design and simulation tools (ADE, Virtuoso, Spectre, etc.). This course will be a great experience for the people who are interested to learn the techniques of Analog IC Design as well.

WHO SHOULD ATTEND

Engineers/ Faculty members/ Students/ Industry personnel who wish to acquire basic knowledge about designing, analysis and simulation of VLSI circuits using Cadence- an industrial EDA tool.

COURSE CONTENTS

- Introduction to VLSI Circuits
- Trends in VLSI Technology
- Introduction to Cadence and its various tools.
- Digital VLSI Design using Cadence
- Analog VLSI Design using Cadence
- VLSI Research Areas

The design flow includes:

- CMOS Analog and Digital design
- Circuit design & Simulation
- Layout design
- DRC/LVS by Assura
- Extraction of RC Components
- Generation of GDSII file

RESOURCE PERSONS

- Dr. Dipankar Pal, Post Doc, BITS Pilani, Goa Campus
- Dr. K.R. Pai, Ex-HOD, ETC Dept., PCCE, Goa
- Mr. Akhilesh Naik, Research scholar, BITS Pilani, Goa campus
- Ms. Rohini Korti, Assistant Professor, ETC Dept, PCCE
- Ms. Reena Fernandes, Assistant Professor, ETC Dept, PCCE

ABOUT CADENCE

Cadence is a leading provider of EDA and semiconductor IP. The custom/analog tools provided by Cadence help engineers design the transistors, standard cells, and IP blocks that make up SoCs. The digital tools automate the design and verification of giga-scale, giga-hertz SoCs at the latest semiconductor processing nodes. The IC packaging and PCB tools permit the design of complete boards and subsystems. Cadence also offers a growing portfolio of design IP and verification IP for memories, interface protocols, analog/mixed-signal components, and specialized processors. And reaching up to the systems level, Cadence offers an integrated suite of hardware/software co-development platforms. In short, Cadence® technology helps customers build great products that connect the world.

PRE-REQUISITES

The programme is open to students, faculty members from all branches and industry personnel with an interest to know about and understand the intrinsics of Analog and digital circuits through high end simulation.

ABOUT THE COLLEGE

P.C.C.E. was established in the year 1997 to meet the growing technical needs of Goa and the country as a whole. The self-financed college, conducts four year degree programmes in Computer, Mechanical , ETC Engineering and Information Technology. The college also offers ME course with specialization in Internet Technology. The college is affiliated to Goa University, Taleigao Plateau, Goa, and all the programmes are approved by All India Council for Technical Education (AICTE), New Delhi.

Website : www.pccegoa.org

(Registration forms can be downloaded here)

Cadence- Design, Analysis and Simulation of Circuits.

APPLICATION FORM

Name : _____

Affiliation:_____

Status (Student/Faculty/Industry) _____

Branch & Roll Number (*for students only*)

_____ _____

IETE/ISTE Membership Number (*for students only*)

_____

Mobile /Landline Number: _____

Email: _____

Name of the institute /Company : _____

_____

Details and Mode of Payment : Draft /Cash

Details of demand draft: _____

Draft Number: _____

Date: _____

Amount: _____

Bank and Branch: _____

_____

Signature of the candidate

Registration Form can be downloaded from the link provided on the college website.

REGISTRATION CHARGES

Faculty/Industry personnel: Rs. 2,500/- (incl. GST)
Student (non-IETE): Rs. 2,250/- (incl. GST)
Student (IETE member): Rs. 2,000/-(incl. GST)

The course fee covers course material and working lunch. Outstation participants will have to arrange for their own accommodation. Help in finding suitable hotels nearby can be provided.

HOW TO APPLY

Send completed application along with demand draft, with appropriate amount, drawn in favor of : *Director, Padre Conceicao College of Engg.,* to: **Prof. Jayalaxmi Devate, HOD - ETC, Padre Conceição College of Engg., Verna, Goa, 403722**.
(Local candidates can pay in cash)
Alternatively, the scanned copy of the form can be sent to : vlsisttp.jan2018pcce@gmail.com

Last date for payment/ applications: **15th Dec. 2017**
NOTE: LIMITED SEATS

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Chief Patron: Rev.Fr. Anthony Castello ,
Director

Patron : Dr. Mahesh Parappagoudar,
Principal

Convenor : Dr. Jayalaxmi Devate,
Head, Department of Electronics & Telecommunication Engineering

Coordinators

Ms.Reena Fernandes (9921712589)
Ms. Rohini Korti (9623630289)
Office: 0832-2791266/67 Extn: 130/157

Department of Electronics and Telecommunication Engineering
Padre Conceição College of Engineering, Verna, Goa

in association with

IETE

(Institution of Electronics and Telecommnication Engineers)

Announces
a ONE WEEK
ISTE STTP
on

"Cadence – Design, Analysis and Simulation of Circuits"

from
01st to 05th January 2018
at
Padre Conceicao College of Engineering, Verna, Goa.